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What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of calibrating a data path of a digital circuit, said method comprising:

clocking an input data signal on said data path into said digital circuit using a clock signal, each bit of said input data signal having a data eye during which said bit is valid;

adjusting the relative timing of said input data signal with respect to said clock signal to position a clocking transition of said clock signal at an edge of said data eye; and

further adjusting the relative timing of said input data signal with respect to said clock signal by moving the data signal relative to the clock signal by a predetermined amount which is approximately equal to one-half of a width of said data eye to position said clocking transition at approximately a center of said data eye.

2. The method of claim 1, wherein said edge is a leading edge and said further adjusting comprises delaying said data signal by said predetermined amount.

3. The method of claim 1, wherein said edge is a trailing edge and said further adjusting comprises advancing said data signal by said predetermined amount.

4. The method of claim 1, wherein said adjusting the relative timing comprises adjusting a delay applied to said data signal until said clocking transition is positioned at said edge.

5. The method of claim 4, wherein said adjusting the relative timing comprises first adjusting said delay of said data signal until a predetermined pattern contained in said data signal is correctly received and then further adjusting said delay of said data signal until said predetermined pattern is no longer received.

6. The method of claim 5, wherein said first adjusting said delay comprises:

a) examining a predetermined number of bits in said data signal for said predetermined pattern;

b) if said predetermined pattern is not found, adjusting the delay applied to said data signal; and

c) repeating steps a) and b) until said predetermined pattern is found in the examined predetermined number of bits.

7. The method of claim 6, wherein said further adjusting said delay comprises:

d) examining a predetermined number of bits in said data signal for said predetermined pattern;

e) if said predetermined pattern is found, adjusting the delay applied to said data signal in a first predetermined direction; and

f) repeating steps d) and e) until said predetermined pattern is no longer found in said data bits.

8. The method of claim 6, wherein said adjusting the delay of act b) comprises:

determining whether said predetermined number of bits in said data signal is shifted right or left as compared with said predetermined pattern; and

adjusting the delay applied to said data signal such that the delay applied to said data signal is subtracted when said predetermined number of bits is shifted right and the delay applied to said data signal is added when said predetermined number of bits is shifted left.

9. The method of claim 8 further comprising:

determining that said predetermined number of bits is shifted right as compared with said predetermined pattern; and

subtracting delay applied to said data signal.

10. The method of claim 8 further comprising:

determining that said predetermined number of bits is shifted left as compared with said predetermined pattern; and

adding delay applied to said data signal.

11. The method of claim 7, wherein said adjusting the delay of act e) comprises:

subtracting delay from said data signal.

12. The method of claim 1, wherein said act of clocking comprises receiving said input data signal at a data input port of a dynamic random access memory.

13. The method of claim 5, wherein said act of adjusting said delay comprises adjusting said delay until a predetermined 4-bit pattern is received.

14. The method of claim 9, wherein said act of determining comprises determining that a received 4-bit pattern is shifted right as compared with a predetermined 4-bit pattern.

15. The method of claim 10, wherein said act of determining comprises determining that a received 4-bit pattern is shifted left as compared with a predetermined 4-bit pattern.

16. A system for calibrating a data path of a digital circuit, said system comprising:

a latch circuit for clocking an input data signal on said data path into said digital circuit using a clock signal, each bit of said input data signal having a data eye during which said bit is valid;

a logic circuit for adjusting the relative timing of said input data signal with respect to said clock signal to position a transition of said clock signal at an edge of a data eye, said logic circuit further adjusting the relative timing of said input data signal with respect to said clock signal by moving the data signal relative to the clock signal by a predetermined amount which is approximately equal to one-half of a width of said data eye to position said clocking transition at approximately a center of said data eye.

17. The system of claim 16 further comprising:

a receiver for receiving said input data signal, and wherein said logic circuit comprises:

a storage device coupled to said receiver for temporarily storing a predetermined number of bits of said input data signal;

an examining device coupled to said storage device for examining said predetermined number of bits of said input data signal for a predetermined bit pattern.

18. The system of claim 17, wherein said receiver comprises an input port of a dynamic random access memory (DRAM).

19. The system of claim 18, wherein said input port comprises a write data input path for data to be written into a memory core.

20. The system of claim 17, wherein said storage device comprises a multi-bit data register.

21. The system of claim 20, wherein said data register contains at least four stages for storing four data bits of said input data signal.

22. The system of claim 17, wherein said examining device comprises a phase detector.

23. The system of claim 17, wherein said examining device comprises a comparator.

24. The system of claim 17, wherein said examining device generates signals indicating when said received pattern does not match said predetermined pattern and further indicating whether a delay applied to a received data signal needs to be increased or decreased, said logic circuit further comprises:

a pass/fail circuit; and

an add/subtract shifter coupled to said pass/fail circuit, said pass/fail circuit being adapted to generate a control signal when said examining device indicates that a received data pattern does not match said predetermined bit pattern, said control signal instructing said add/subtract shifter to add or subtract a delay applied to a received input data signal.

25. The system of claim 24, wherein said add/subtract shifter is coupled to:

said delay circuit for instructing said delay circuit to add/subtract said delay applied to said received input data signal; and

said delay circuit is also coupled to said pass/fail circuit for receiving a control signal from said pass/fail circuit when said received input data signal matches said predetermined bit pattern, said delay circuit being configured to add a delay to said received input data signal that is approximately equal to one-half of the duration of said data eye.

26. The system of claim 24, wherein said add/subtract shifter is coupled to a first adjustable delay circuit for instructing said first delay circuit to add/subtract said delay applied to said received input data signal.

27. The system of claim 26 further comprising a second delay circuit coupled to said pass/fail circuit for receiving a control signal from said pass/fail circuit when said received input data signal matches said predetermined bit pattern, said

delay circuit being configured to add a delay to said received input data signal that is approximately equal to one-half of the duration of said data eye.

28. The system of claim 25, wherein said data eye has a duration of approximately 0.25 ns.

29. The system of claim 17 further comprising a controller for driving said input data signal received on said write data input path.

30. The system of claim 26, wherein said examining device comprises:

a first NAND gate, a first input of which is a first bit of said received input data signal, a second input of which is an inverse of a second bit of said received input data signal;

a second NAND gate, a first input of which is an inverse of a third bit of said received input data signal, a second input of which is a fourth bit of said received input data signal;

a first NOR gate, wherein an output of said first and second NAND gates are coupled to respective inputs of said first NOR gate, said first NOR gate producing an output ADD when said received input data signal is shifted left as compared with said predetermined bit pattern;

a third NAND gate, a first input of which is an inverse of said first bit of said received input data signal, a second input of which is said second bit of said received input data signal;

a fourth NAND gate, a first input of which is said third bit of said received input data signal, a second input of which is an inverse of said fourth bit of said received input data signal; and

a second NOR gate, wherein an output of said third and fourth NAND gates are coupled to respective inputs of said second NOR gate, said second NOR gate producing an output SUBTRACT when said received data signal is shifted right as compared with said predetermined bit pattern.

31. The system of claim 30, wherein said pass/fail circuit comprises:

a third NOR gate for receiving said ADD and SUBTRACT outputs of said first and second NOR gates;

a latch coupled to an output of said third NOR gate, said latch producing an output PASS when said received data signal matches said predetermined bit pattern;

a fifth NAND gate for receiving said respective ADD and PASS outputs of said first NOR gate and said latch, said fifth NAND gate producing an output for instructing said adjustable delay circuit to add a delay; and

a sixth NAND gate for receiving said SUBTRACT output of said second NOR gate and a PASS inverse output of said latch, said sixth NAND gate producing an output for instructing said adjustable delay circuit to subtract a delay.

32. The system of claim 31, wherein said predetermined bit pattern is a 4-bit pattern.

33. An integrated circuit semiconductor device comprising a system for calibrating a data path of a digital circuit, said system comprising:

a latch circuit for clocking an input data signal on said data path into said digital circuit using a clock signal, each bit of said input data signal having a data eye during which said bit is valid;

a logic circuit for adjusting the relative timing of said input data signal with respect to said clock signal to position a transition of said clock signal at an edge of a data eye, said logic circuit further adjusting the relative timing of said input data signal with respect to said clock signal by moving the data signal relative to the clock signal by a predetermined amount which is approximately equal to one-half of a width of said data eye to position said clocking transition at approximately a center of said data eye.

34. The integrated circuit device of claim 33, wherein said system further comprises:

a receiver for receiving said input data signal, and wherein said logic circuit comprises:

a storage device coupled to said receiver for temporarily storing a predetermined number of bits of said input data signal;

an examining device coupled to said storage device for examining said predetermined number of bits of said input data signal for a predetermined bit pattern.

35. The integrated circuit device of claim 34, wherein said receiver comprises an input port of a dynamic random access memory (DRAM).

36. The integrated circuit device of claim 35, wherein said input port comprises a write data input path for data to be written into a memory core.

37. The integrated circuit device of claim 34, wherein said storage device comprises a multi-bit data register.

38. The integrated circuit device of claim 37, wherein said data register contains at least four stages for storing four data bits of said input data signal.

39. The integrated circuit device of claim 34, wherein said examining device comprises a phase detector.

40. The integrated circuit device of claim 34, wherein said examining device comprises a comparator.

41. The integrated circuit device of claim 34, wherein said examining device generates signals indicating when said received pattern does not match said predetermined pattern and further indicating whether a delay applied to a received data signal needs to be increased or decreased, said logic circuit further comprises:

a pass/fail circuit; and

an add/subtract shifter coupled to said pass/fail circuit, said pass/fail circuit being adapted to generate a control signal when said examining device indicates that a received data pattern does not match said predetermined bit pattern, said control signal instructing said add/subtract shifter to add or subtract a delay applied to a received input data signal.

42. The integrated circuit device of claim 41, wherein said add/subtract shifter is coupled to:

said delay circuit for instructing said delay circuit to add/subtract said delay applied to said received input data signal; and

said delay circuit is also coupled to said pass/fail circuit for receiving a control signal from said pass/fail circuit when said received input data signal matches said predetermined bit pattern, said delay circuit being configured to add a delay to said received input data signal that is approximately equal to one-half of the duration of said data eye.

43. The integrated circuit device of claim 41, wherein said add/subtract shifter is coupled to a first adjustable delay circuit for instructing said first delay circuit to add/subtract said delay applied to said received input data signal.

44. The integrated circuit device of claim 43, wherein said system further comprises a second delay circuit coupled to said pass/fail circuit for receiving a control signal from said pass/fail circuit when said received input data signal matches said predetermined bit pattern, said delay circuit being configured to add a delay to said received input data signal that is approximately equal to one-half of the duration of said data eye.

45. The integrated circuit device of claim 42, wherein said data eye has a duration of approximately 0.25 ns.

46. The integrated circuit device of claim 34, wherein said system further comprises a controller for driving said data pattern received on said write data input path.

47. The integrated circuit device of claim 43, wherein said examining device comprises:

a first NAND gate, a first input of which is a first bit of said received input data signal, a second input of which is an inverse of a second bit of said received input data signal;

a second NAND gate, a first input of which is an inverse of a third bit of said received input data signal, a second input of which is a fourth bit of said received input data signal;

a first NOR gate, wherein an output of said first and second NAND gates are coupled to respective inputs of said first NOR gate, said first NOR gate producing an output ADD when said received input data signal is shifted left as compared with said predetermined bit pattern;

a third NAND gate, a first input of which is an inverse of said first bit of said received input data signal, a second input of which is said second bit of said received input data signal;

a fourth NAND gate, a first input of which is said third bit of said received input data signal, a second input of which is an inverse of said fourth bit of said received input data signal; and

a second NOR gate, wherein an output of said third and fourth NAND gates are coupled to respective inputs of said second NOR gate, said second NOR gate producing an output SUBTRACT when said received data signal is shifted right as compared with said predetermined bit pattern.

48. The integrated circuit device of claim 47, wherein said pass/fail circuit comprises:

a third NOR gate for receiving said ADD and SUBTRACT outputs of said first and second NOR gates;

a latch coupled to an output of said third NOR gate, said latch producing an output PASS when said received data signal matches said predetermined bit pattern;

a fifth NAND gate for receiving said respective ADD and PASS outputs of said first NOR gate and said latch, said fifth NAND gate producing an output for instructing said adjustable delay circuit to add a delay; and

a sixth NAND gate for receiving said SUBTRACT output of said second NOR gate and a PASS inverse output of said latch, said sixth NAND gate producing an output for instructing said adjustable delay circuit to subtract a delay.

49. A processor system comprising:

a processor; and

a dynamic random access memory (DRAM) coupled to said processor, at least one of said processor and memory having a system for calibrating a data path of a digital circuit, said system for calibrating comprising:

a latch circuit for clocking an input data signal on said data path into said digital circuit using a clock signal, each bit of said input data signal having a data eye during which said bit is valid;

a logic circuit for adjusting the relative timing of said input data signal with respect to said clock signal to position a transition of said clock signal at an edge of a data eye, said logic circuit further adjusting the relative timing of said input data signal with respect to said clock signal by moving the data signal

relative to the clock signal by a predetermined amount which is approximately equal to one-half of a width of said data eye to position said clocking transition at approximately a center of said data eye.

50. The processor system of claim 49, wherein said system for calibrating further comprises:

a receiver for receiving said input data signal;

a storage device coupled to said receiver for temporarily storing a predetermined number of bits of said input data signal;

an examining device coupled to said storage device for examining said predetermined number of bits of said input data signal for a predetermined bit pattern.

51. The processor system of claim 50, wherein said receiver comprises an input port of said dynamic random access memory (DRAM).

52. The processor system of claim 51, wherein said input port comprises a write data input path for data to be written into a memory core.

53. The processor system of claim 50, wherein said storage device comprises a multi-bit data register.

54. The processor system of claim 53, wherein said data register contains at least four stages for storing four data bits of said input data signal.

55. The processor system of claim 50, wherein said examining device comprises a phase detector.

56. The processor system of claim 50, wherein said examining device comprises a comparator.

57. The processor system of claim 50, wherein said system for calibrating further comprises:

a pass/fail circuit; and

an add/subtract shifter coupled to said pass/fail circuit, said pass/fail circuit being adapted to generate a control signal when said examining device indicates that a received data pattern does not match said predetermined bit pattern, said control signal instructing said add/subtract shifter to add or subtract a delay applied to a received input data signal.

58. The processor system of claim 57, wherein said add/subtract shifter is coupled to:

said delay circuit for instructing said delay circuit to add/subtract said delay applied to said received input data signal; and

said delay circuit is also coupled to said pass/fail circuit for receiving a control signal from said pass/fail circuit when said received input data signal matches said predetermined bit pattern, said delay circuit being configured to add a delay to said received input data signal that is approximately equal to one-half of the duration of said data eye.

59. The processor system of claim 58, wherein said system for calibrating further comprises a first adjustable delay circuit for instructing said first delay circuit to add/subtract said delay applied to said received input data signal.

60. The processor system of claim 59, wherein said system for calibrating further comprises a second delay circuit coupled to said pass/fail circuit for receiving a control signal from said pass/fail circuit when said input data signal matches said predetermined bit pattern, said delay circuit being configured to add a delay to said received input data signal that is approximately equal to one-half of the duration of said data eye.

61. The processor system of claim 49, wherein said processor has said system for calibrating.

62. The processor system of claim 49, wherein said memory has said system for calibrating.

63. The processor system of claim 60, wherein said data eye has a duration of approximately 0.25 ns.

64. The processor system of claim 60, wherein said system for calibrating further comprises a controller for driving said input data signal received on said write data input path.

65. The processor system of claim 59, wherein said phase detector comprises:

a first NAND gate, a first input of which is a first bit of said received input data signal, a second input of which is an inverse of a second bit of said received input data signal;

a second NAND gate, a first input of which is an inverse of a third bit of said received input data signal, a second input of which is a fourth bit of said received input data signal;

a first NOR gate, wherein an output of said first and second NAND gates are coupled to respective inputs of said first NOR gate, said first NOR gate producing an output ADD when said received input data signal is shifted left as compared with said predetermined bit pattern;

a third NAND gate, a first input of which is an inverse of said first bit of said received input data signal, a second input of which is said second bit of said received input data signal;

a fourth NAND gate, a first input of which is said third bit of said received input data signal, a second input of which is an inverse of said fourth bit of said received input data signal; and

a second NOR gate, wherein an output of said third and fourth NAND gates are coupled to respective inputs of said second NOR gate, said second NOR gate producing an output SUBTRACT when said received data signal is shifted right as compared with said predetermined bit pattern.

66. The processor system of claim 65, wherein said pass/fail circuit comprises:

a third NOR gate for receiving said ADD and SUBTRACT outputs of said first and second NOR gates;

a latch coupled to an output of said third NOR gate, said latch producing an output PASS when said received data signal matches said predetermined bit pattern;

a fifth NAND gate for receiving said respective ADD and PASS outputs of said first NOR gate and said latch, said fifth NAND gate producing an output for instructing said adjustable delay circuit to add a delay; and

a sixth NAND gate for receiving said SUBTRACT output of said second NOR gate and a PASS inverse output of said latch, said sixth NAND gate producing an output for instructing said adjustable delay circuit to subtract a delay.